

Preliminary Technical Data

ADG701/702

FEATURES

+1.8V to +5.5V Single Supply

1 Ω On Resistance

Low On-Resistance Flatness

Bandwidth 100MHz

Rail to Rail Operation

Very Low Distortion

6-lead SOT-23

8-lead μ SOIC Packages

Fast Switching Times

t_{ON} 20 ns

t_{OFF} 10 ns

Low Power Consumption (1 μ W)

TTL/CMOS Compatible

APPLICATIONS

Battery Powered Systems

Communication Systems

Sample Hold Systems

Audio Signal Routing

Video

Mechanical Reed Relay Replacement

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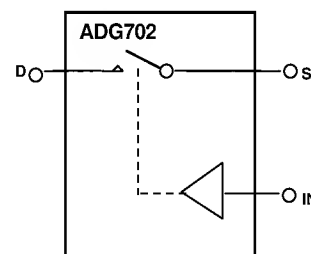
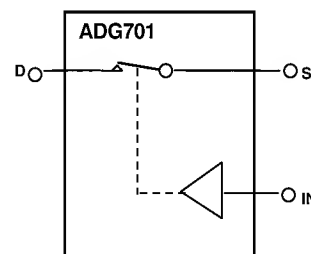
GENERAL DESCRIPTION

The ADG701/702 are monolithic CMOS SPST switches. These switches are designed on an advanced sub-micron process which provides low power dissipation yet gives high switching speed, low on resistance and low leakage currents.

The ADG701/702 can operate from a single +1.8V to +5.5V supply making it ideal for use in battery powered instruments, and with the new generation of DACs and ADCs from Analog Devices.

Each switch conducts equally well in both directions when ON.

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT HIGHLIGHTS

1. +2V/+3V/+5V Single Supply Operation. The ADG701/702 offer high performance, including low on resistance and fast switching times and is fully specified and guaranteed with +3V and +5V supply rails.
2. Low R_{ON} (4 Ω max, 1 Ω typ).
3. Bandwidth 100MHz
4. Low power dissipation
CMOS construction ensures low power dissipation.
5. Fast T_{ON}/T_{OFF}
6. Tiny 6-lead SOT-23 and 8-lead μ SOIC.

PrelimB. 11/97

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Parameter	B Version		Units	Test Conditions/Comments
	+25°C	$-40^{\circ}C$ to $+85^{\circ}C$		
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}		V
On-Resistance (R_{ON})	1	1.5 2.5	Ω typ Ω max	$V_S = 0V$ to 5V
On-Resistance Match Between Channels (ΔR_{ON})		1.0	Ω typ Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)		1.0	Ω max	Ω typ
LEAKAGE CURRENTS				TBD
Source OFF Leakage I_S (OFF)		2.0	nA typ nA max	
Drain OFF Leakage I_D (OFF)		2.0	nA typ nA max	
Channel ON Leakage I_D , I_S (ON)		4.0	nA typ nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current I_{INL} or I_{INH}	0.005	± 0.5	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
DYNAMIC CHARACTERISTICS ²				TBD
t_{ON}		20	ns max	
t_{OFF}		10	ns max	
Charge Injection	10		pC typ	
Bandwidth -3 dB	100		MHz typ	
Bandwidth ± 0.1 dB	TBD		MHz typ	
Off Isolation	80		dB typ	
C_S (OFF)	TBD		pF typ	
C_D (OFF)	TBD		pF typ	
C_D , C_S (ON)	TBD		pF typ	
POWER REQUIREMENTS				$V_{DD} = +5V$ Digital Inputs = 0 V or 5 V
I_{DD}	0.0001	0.5	μA typ μA max	

NOTES

¹Temperature ranges are as follows: B Versions: $-40^{\circ}C$ to $+85^{\circ}C$.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG701/702—SPECIFICATIONS¹

(V_{DD} = 2.7V to 3.6V, GND = 0 V. All specifications -40°C to +85°C, unless otherwise noted.)

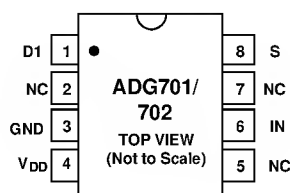
Parameter	B Version		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V _{DD}		V
On-Resistance (R _{ON})	2	3 4	Ω typ Ω max	V _S = 0V to 3V
On-Resistance Match Between Channels (ΔR _{ON})		1.0	Ω typ Ω max	
On-Resistance Flatness (R _{FLAT(ON)})		2.0	Ω max	Ω typ
LEAKAGE CURRENTS				TBD
Source OFF Leakage I _S (OFF)		2.0	nA typ nA max	
Drain OFF Leakage I _D (OFF)		2.0	nA typ nA max	
Channel ON Leakage I _D , I _S (ON)		4.0	nA typ nA max	
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.0	V min	
Input Low Voltage, V _{INL}		0.4	V max	
Input Current I _{INL} or I _{INH}	0.005	±0.5	μA typ μA max	V _{IN} = V _{INL} or V _{INH}
DYNAMIC CHARACTERISTICS ²				TBD
t _{ON}		30	ns max	
t _{OFF}		15	ns max	
Charge Injection	5		pC typ	
Bandwidth -3dB	110		MHz typ	
Bandwidth ± 0.1dB	TBD		MHz typ	
Off Isolation	80		dB typ	
C _S (OFF)	TBD		pF typ	
C _D (OFF)	TBD		pF typ	
C _D , C _S (ON)	TBD		pF typ	
POWER REQUIREMENTS				V _{DD} = +3 V Digital Inputs = 0 V or 3 V
I _{DD}	0.0001	0.5	μA typ μA max	

NOTES

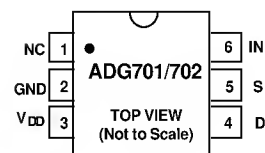
¹Temperature ranges are as follows: B Versions: -40°C to +85°C.²Guaranteed by design, not subject to production test.

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PIN CONFIGURATION (MICRO SOIC)



PIN CONFIGURATION (SOT-23)



ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

V_{DD} to GND -0.3 V to +7 V

Analog, Digital Inputs² -0.3V to V_{DD} +0.3 V or
30 mA, Whichever Occurs First

(Pulsed at 1 ms, 10% Duty Cycle max)

Operating Temperature Range

Industrial (B Version) -40°C to +85°C

Storage Temperature Range -65°C to +150°C

Junction Temperature +150°C

MicroSOIC Package, Power Dissipation 450 mW

θ_{JA} Thermal Impedance 206°C/W

θ_{JC} Thermal Impedance 44°C/W

Lead Temperature, Soldering

Vapor Phase (60 sec) +215°C

Infrared (15 sec) +220°C

SOT-23 Package, Power Dissipation TBD mW

θ_{JA} Thermal Impedance 229.6°C/W

θ_{JC} Thermal Impedance 91.99°C/W

Lead Temperature, Soldering

Vapor Phase (60 sec) +215°C

Infrared (15 sec) +220°C

ESD 2kV

NOTES

¹Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

Model ¹	Temperature Range	Package Option ¹
ADG701BRT	-40°C to +85°C	RT-6
ADG702BRT	-40°C to +85°C	RT-6
ADG701BRM	-40°C to +85°C	RM-8
ADG702BRM	-40°C to +85°C	RM-8

NOTES

¹RT = SOT-23; RM = microSOIC.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG701/702 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

V_{DD}	Most positive power supply potential.	C_D (OFF)	“OFF” switch drain capacitance.
		C_D, C_S (ON)	“ON” switch capacitance.
GND	Ground (0 V) reference.	t_{ON}	Delay between applying the digital control input and the output switching on. See test circuit 4.
S	Source terminal. May be an input or output.	t_{OFF}	Delay between applying the digital control input and the output switching off.
D	Drain terminal. May be an input or output.		
IN	Logic control input.	Off Isolation A	A measure of unwanted signal coupling through an “OFF” switch.
R_{ON}	Ohmic resistance between D and S.	Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
ΔR_{ON}	On resistance match between any two channels i.e. $R_{ONmax} - R_{ONmin}$.		
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.		
I_S (OFF)	Source leakage current with the switch “OFF.”		
I_D (OFF)	Drain leakage current with the switch “OFF.”		
I_D, I_S (ON)	Channel leakage current with the switch “ON.”		
V_D (V_S)	Analog voltage on terminals D, S.		
C_S (OFF)	“OFF” switch source capacitance.		

Dimensions are shown in inches and (mm).

Figure 1 shows the dimensions of the test fixture. The dimensions are provided in both inches and millimeters.

Top View Dimensions:

- Pin Pitch (Top): 0.122 (3.10) and 0.114 (2.90)
- Pin Pitch (Bottom): 0.122 (3.10) and 0.114 (2.90)
- Pin Pitch (Left): 0.122 (3.10) and 0.114 (2.90)
- Pin Pitch (Right): 0.122 (3.10) and 0.114 (2.90)
- Pin Diameter: 0.0256 (0.65) BSC
- Overall Width: 0.199 (5.05) and 0.187 (4.75)
- Overall Height: 0.199 (5.05) and 0.187 (4.75)

Side View Dimensions:

- Component Height: 0.043 (1.09)
- Base Thickness: 0.006 (0.15)
- Base Thickness (Alternative): 0.002 (0.05)

Front View Dimensions:

- Component Width: 0.120 (3.05) and 0.112 (2.84)
- Component Height: 0.043 (1.09)
- Base Thickness: 0.003 (0.08)
- Base Thickness (Alternative): 0.002 (0.05)
- Seating Plane: Indicated by an arrow pointing to the base.

Figure 1: Mechanical drawing of the connector. The drawing shows two views of a 6-pin connector. The top view is a plan view showing a rectangular body with six pins. Dimensions include overall width 0.122 (3.10), pin pitch 0.106 (2.70), and pin diameter 0.071 (1.80). The bottom view is a side view showing the profile of the connector. Dimensions include overall height 0.051 (1.30), pin height 0.057 (1.45), and pin diameter 0.035 (0.90). A 'SEATING PLANE' is indicated. A table of dimensions is provided at the bottom right.

Dimension	Value	Value	Value
0.009	(0.23)	0	0.022 (0.55)
0.003	(0.08)	0	0.014 (0.35)